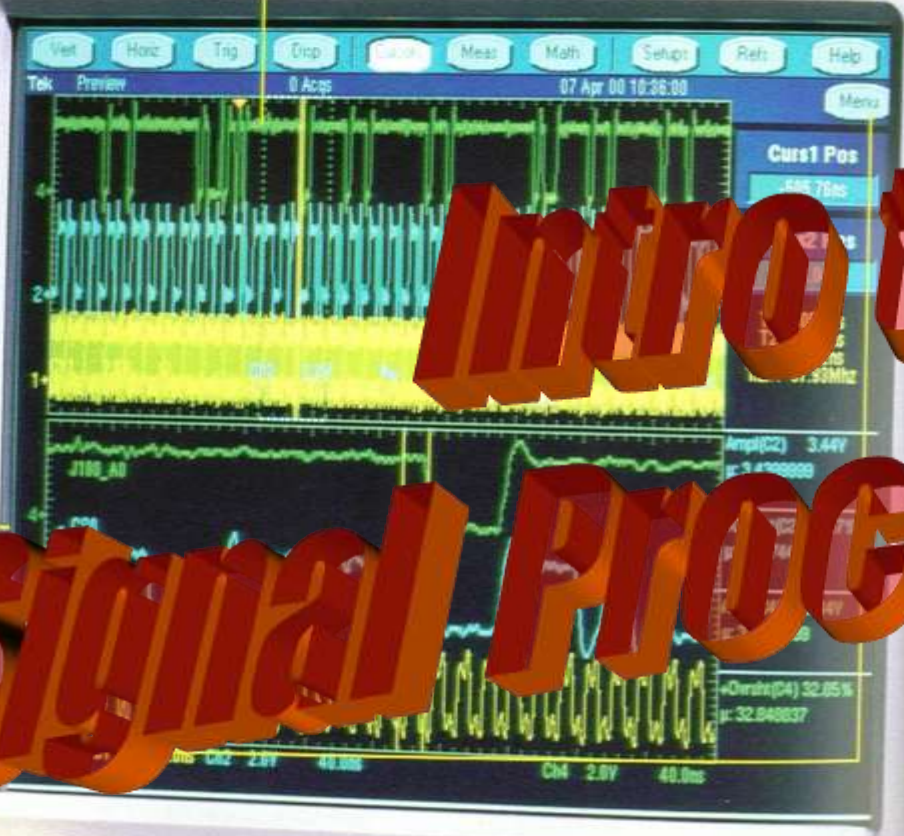


Tektronix TDS 7404 Digital Phosphor Oscilloscope

4 GHz  
20 GS/s DPO



# Intro to Signal Processing

The control panel features several sections of controls:

- HORIZONTAL POSITION:** Includes buttons for FINE, AUTOSET, RECALL, FRONT, DISPRE, FastAcq, and a knob for DELAY.
- TRIGGER:** Includes buttons for EDGE, ADVANCE, RUN STOP, and SINGLE.
- RESOLUTION:** Includes a ZOOM knob and buttons for CH1, CH2, CH3, CH4, EXT, and ARM.
- CH2, CH3, CH4:** Each channel has a POSITION knob and a SCALE knob.

The bottom panel includes several ports and connectors:

- PROBE COMPENSATION: SIGNAL, GND, ADJUST, and AT 100k.
- AUX IN, AUX OUT, and SIGNAL OUT ports.
- Two BNC connectors with cables plugged in.
- A Tektronix TCA-SMA connector.

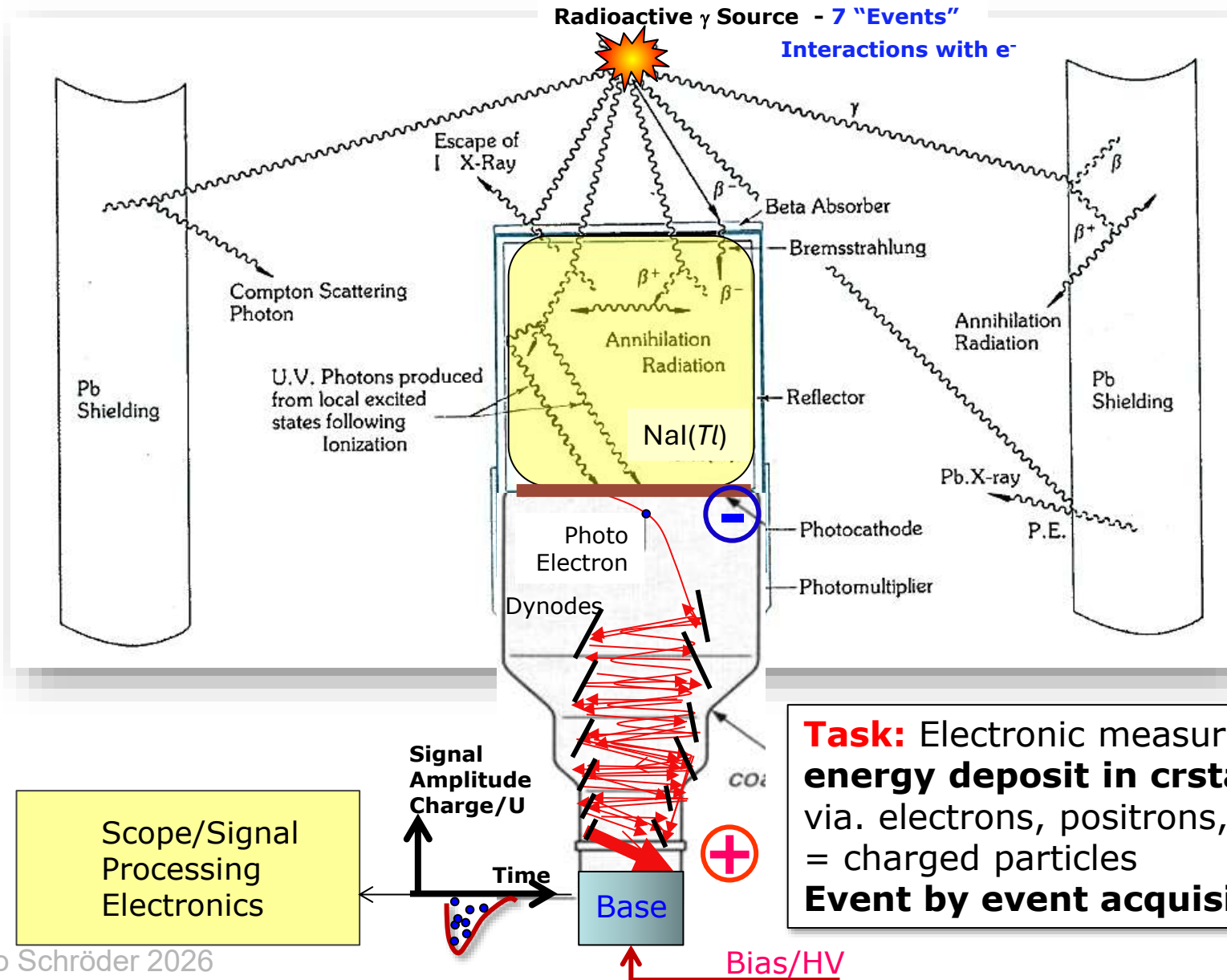
# Agenda

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- *Photon environment, NaI scintillation detectors*
- *Electronic data acquisition setup*  
*Fast-slow signal branches*  
*Scope, PMT signals*  
*Amplifier and discriminator (TSCA),*  
*Functionality*
- ANSEL DDC8 Digital Signal Processor  
Analog-to-digital (ADC) conversion  
Event file structure  
Pulse-height spectrum  
Energy calibration
- Practice detector setup, initial tuning

→ Take Radiation-Safety class/exam

# $\gamma$ Environment in Scintillation Measurements



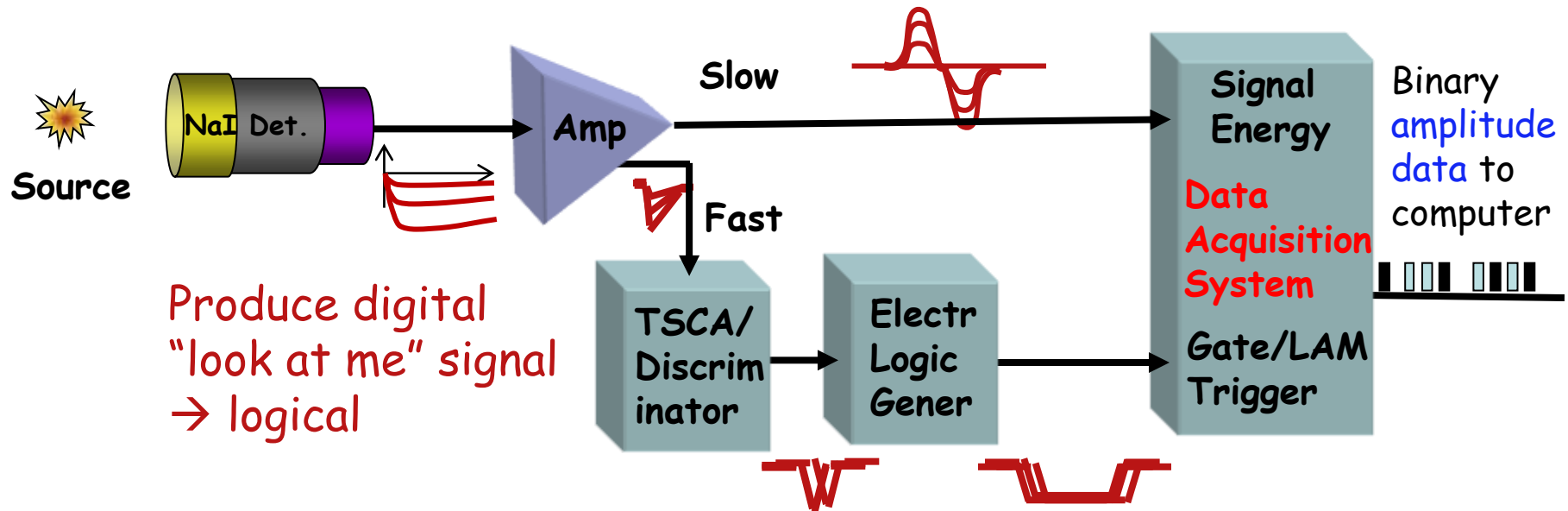
ANSEL L--3 Electronics 3

# Principle of Fast-Slow Signal Processing

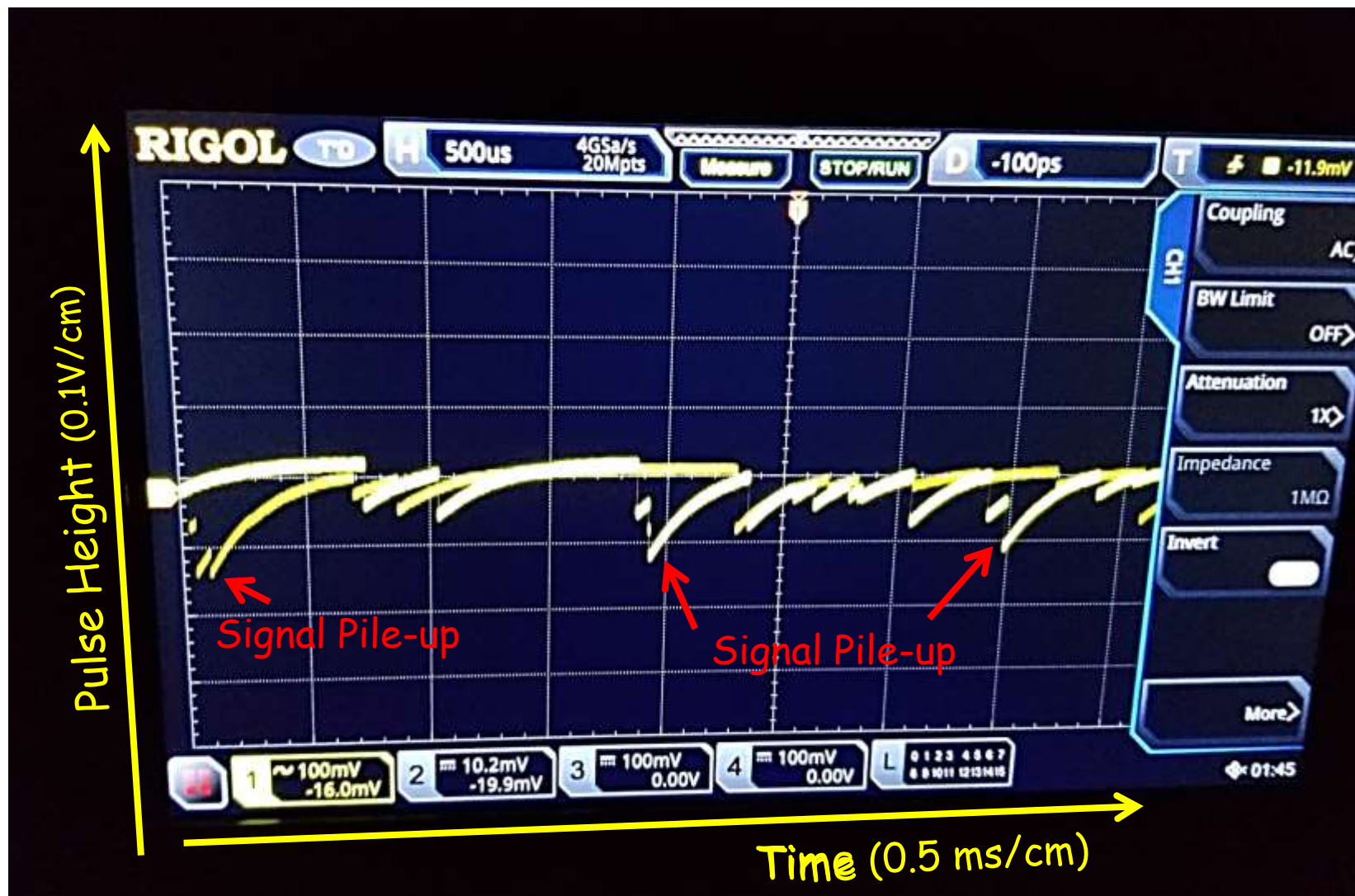
Two branches of signal processing:

1. Fast logic branch: Produce unitary, "logical" signal indicating that detector had one acceptable event, further use in fast decision making (accept/reject)
2. Slow analog branch: Integrate, amplify, and shape original detector energy signal to match requirements of analytical electronics modules and computer data acquisition/storage system.

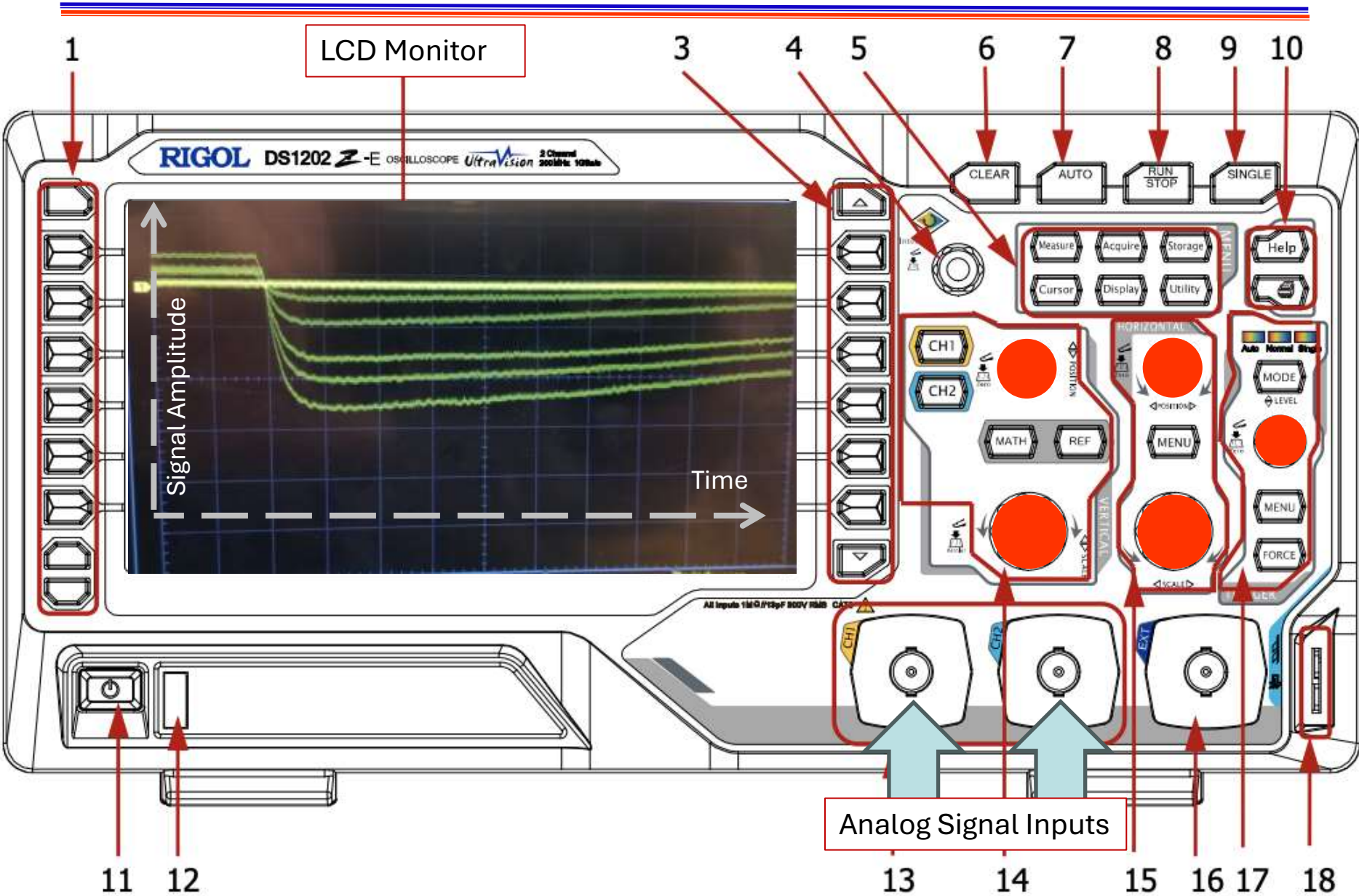
Produce analog signal proportional to energy deposit →



# Signal Pulses: Output from PM Base



# Signal Oscilloscope Front Panel



# Signal Oscilloscope Front Panel Descriptions

No.	Description	No.	Description
1	Measurement Menu Softkeys	10	Help/Print
2	LCD	11	Power Key
3	Function Menu Softkeys	12	USB Host Interface
4	Multifunction Knob	13	Analog Channel Input Area
5	Common Operation Keys	14	VERTICAL Control Area
6	CLEAR	15	HORIZONTAL Control Area
7	AUTO	16	External Trigger Input
8	RUN/STOP	17	TRIGGER Control Area
9	SINGLE	18	Probe Compensation Signal Output Terminal/Ground Terminal

Terminate input signal by 50Ω for NIM logic pulses.

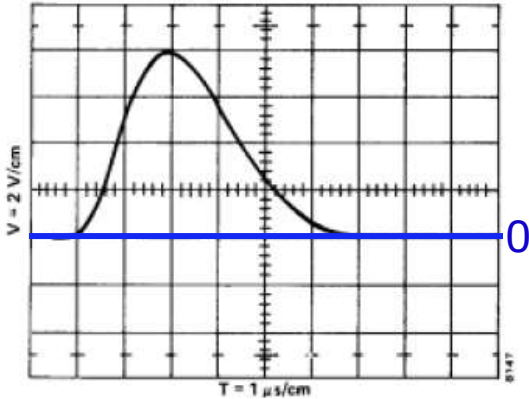
Trigger Menu for time sweep condition: Trigger channel #, rising/falling level, AC vs. DC.

Adjust display ranges and zero for horizontal (time) and vertical (signal amplitude) scale.

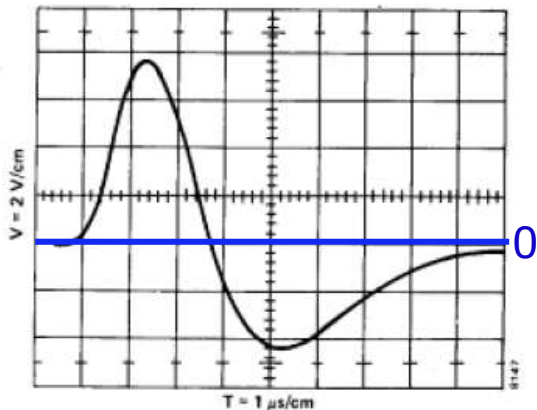
Adjust trigger signal (discriminator) level.

# Analog Branch Elements: Slow Analog Signal Amplifiers

Uniform signal shape for all → Amplitude ~ Energy



Correct Amplifier Unipolar Output.



Correct Amplifier Bipolar Output.



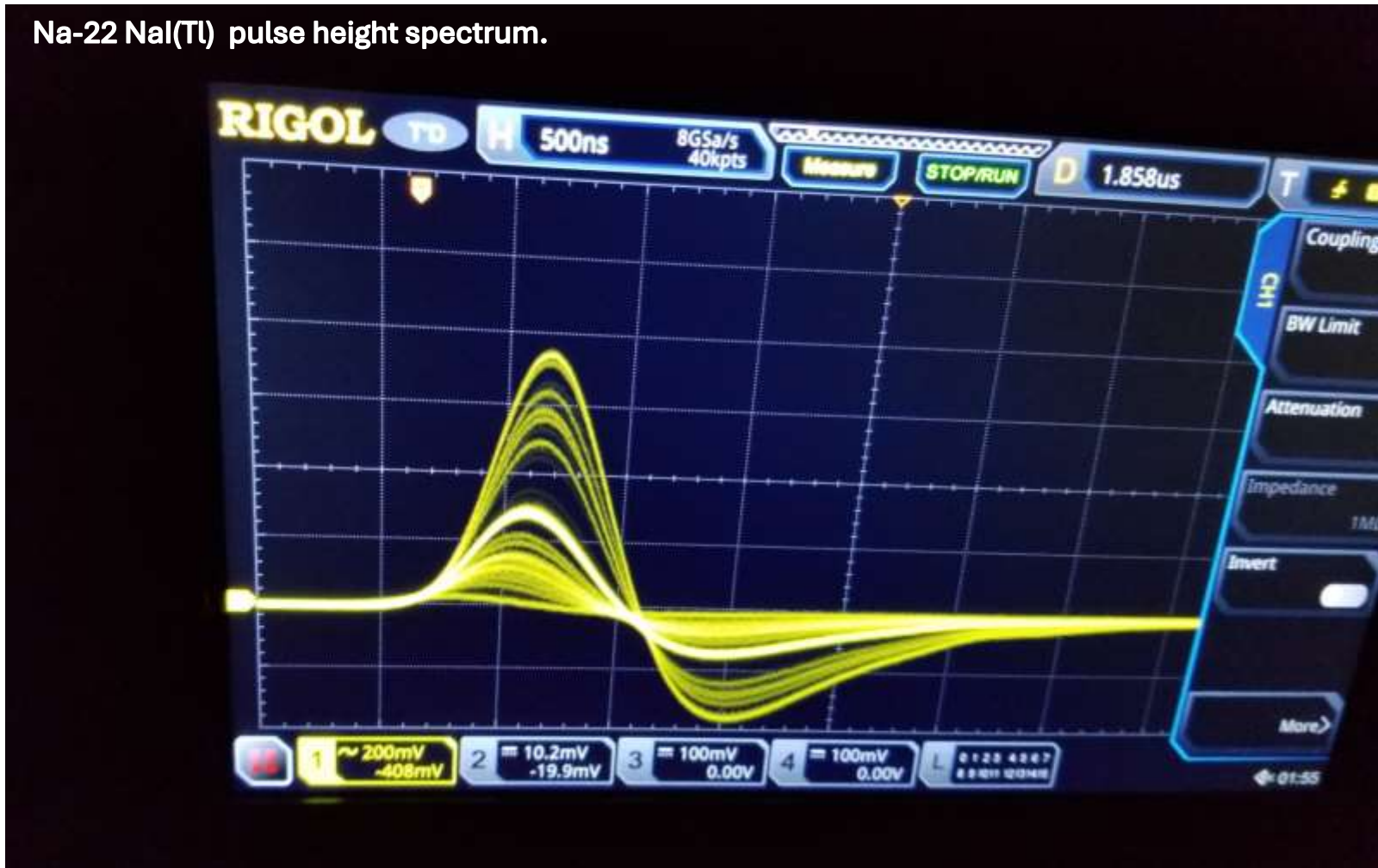
**Tasks:** Generate signal with amplitude proportional to collected detector charge. Needs absolute calibration of pulse amplitude.



← Preamp Power

# Signal Output Main Amplifier

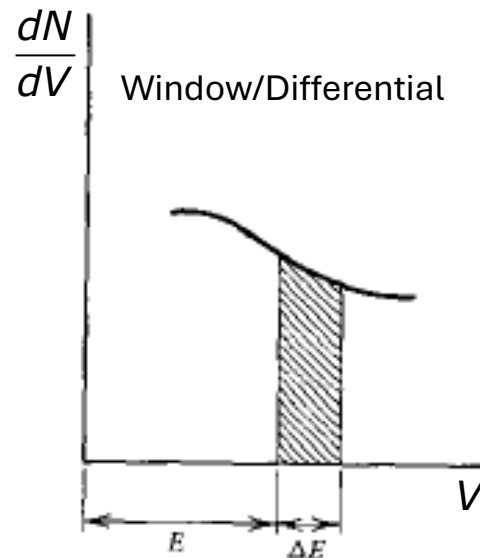
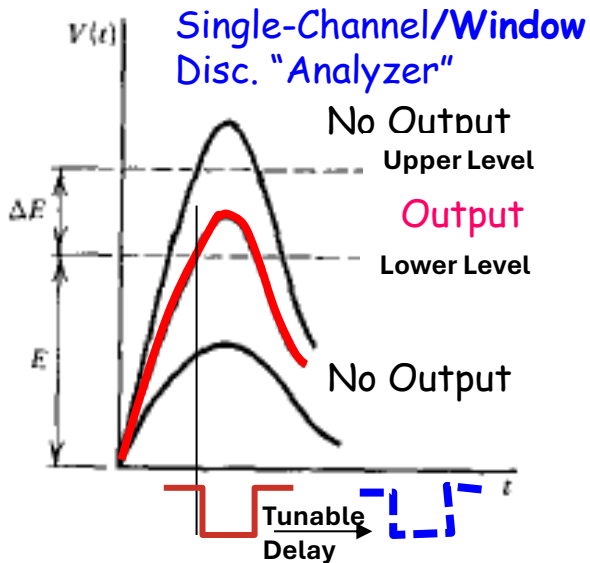
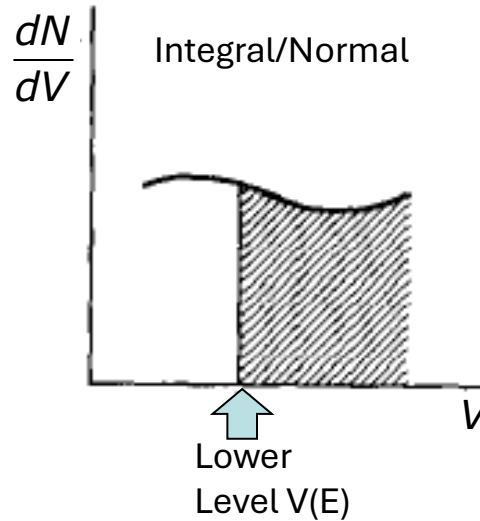
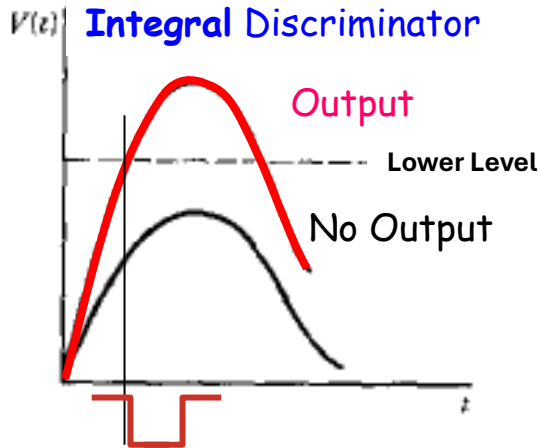
Na-22 NaI(Tl) pulse height spectrum.



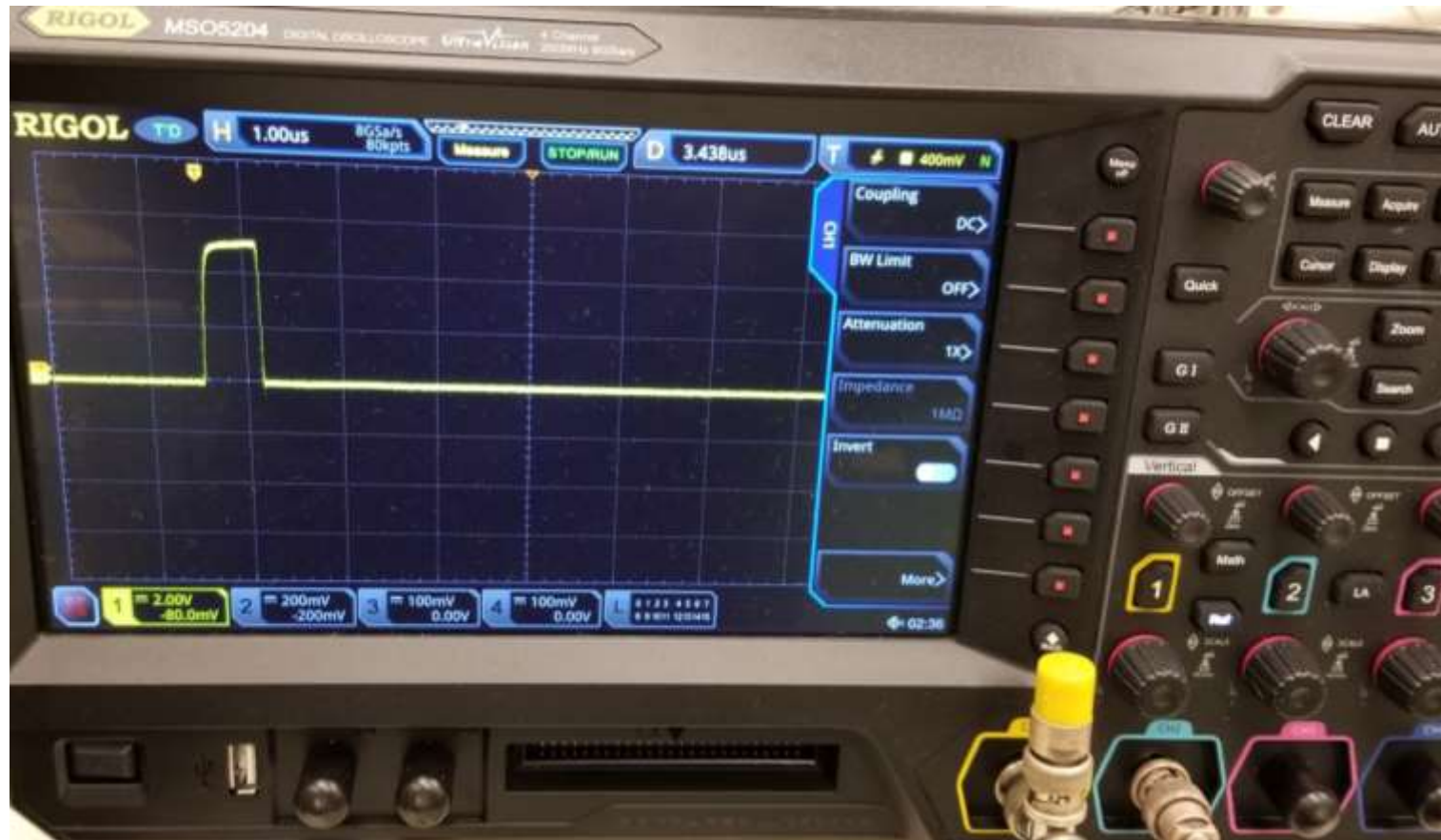
NaI(Tl) detector with Na-22 source. Display of a superposition of several 10s of individual events: Amplifier signal amplitude (200mV/cm) vs. time (500ns/cm).

# Leading-Edge $E$ Discriminator: "Single Channel" TSCA

Tasks: Indicate acceptable event, define "time-zero"  $t_0$



# Logic Branch: NIM/TTL Signals



Logic signals = Discriminator output pulses, have a constant shape, independent of shape and amplitude of input signals from detector.

# Digital Sampling Oscilloscope

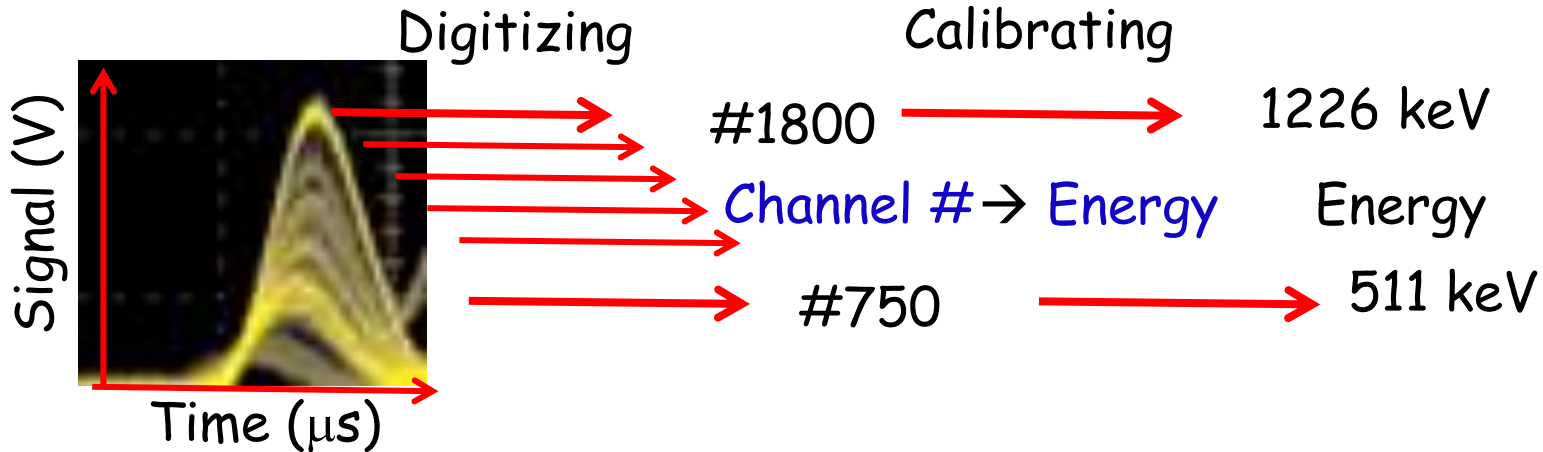
Displaying the time dependent signal amplitude  $U(t)$   
Sweep an illuminated trace  $U(t)$  horizontally along the screen

Signal Trigger Level Adjust

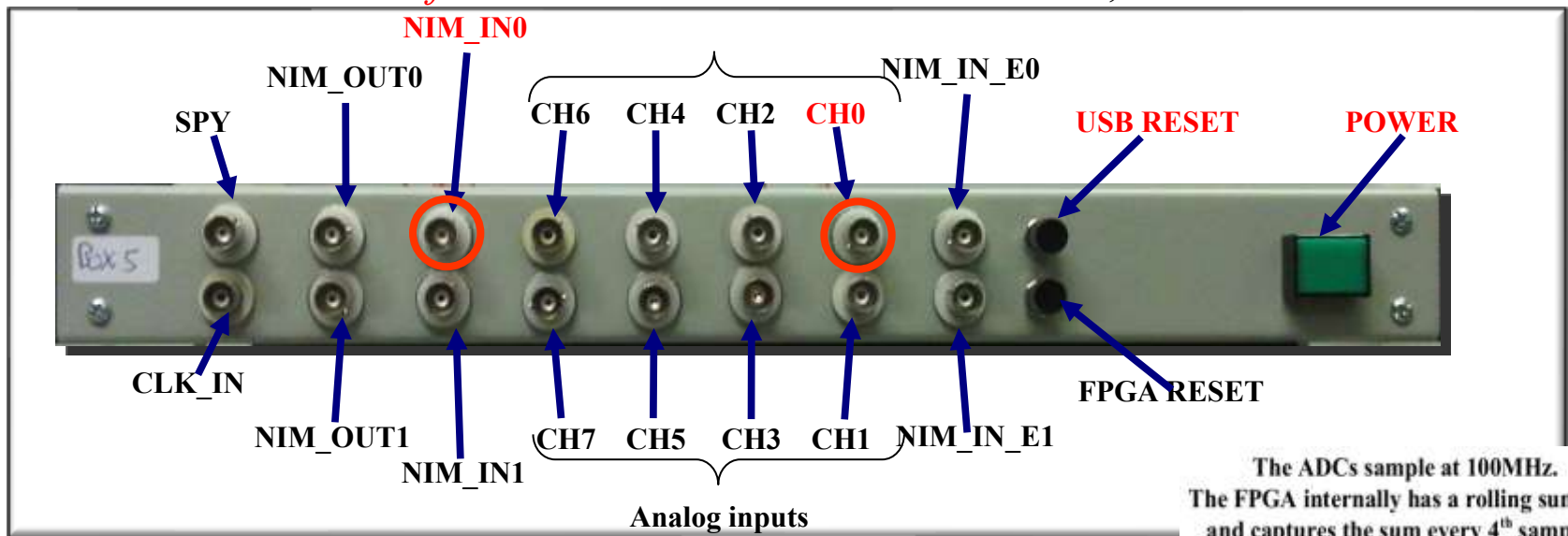


Output media for screen  
shots (USB/Disc)

# Data Acquisition with DDC-8 Digitizer



$2048 = 2^{11} \rightarrow +2V \hat{=} \text{full scale} \rightarrow +1.0V \hat{=} 10\,000\,000\,000, +1.5V \hat{=} 11\,000\,000\,000$

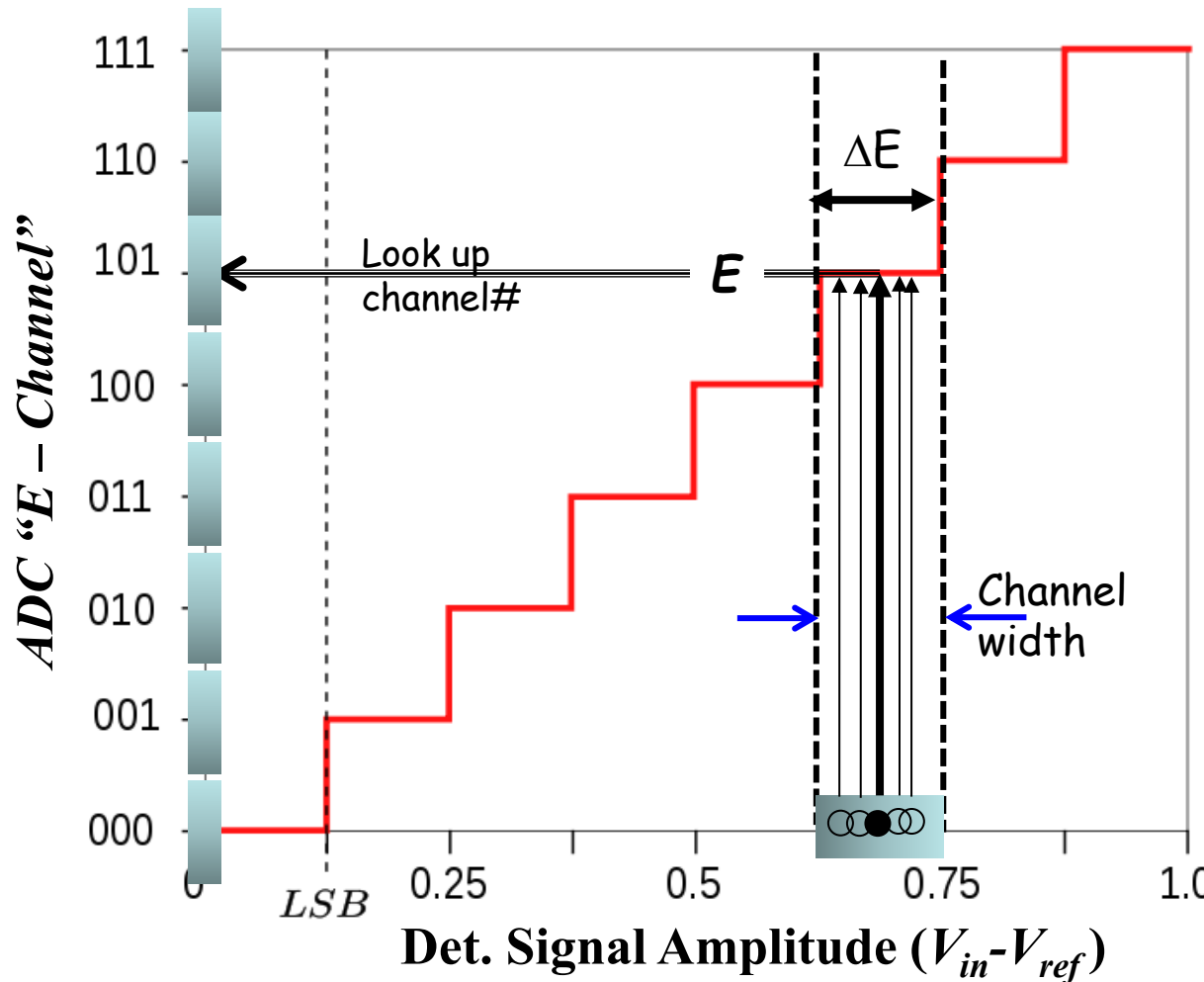


**+/- 1V (maximum amplitude = 2V !!)**

The ADCs sample at 100MHz.  
The FPGA internally has a rolling sum of 4 and captures the sum every 4<sup>th</sup> sample.

Effective sampling = 25MHz  
(1 sample covers 40ns)

# Analog-to-Digital Converter (ADC) Principle of Operation



Divide total range of signal amplitudes into ADC "E channels" (bins) of fixed width  $\Delta E$   $\rightarrow$  event counters. Input signal triggers (initiates) comparator channel scan.

More bins  $\rightarrow$  higher resolution

Typical # of channels per ADC: 1k=1024  
2k,..., 8k.

Event signal amplitude  $\rightarrow$  binary number = ADC#  $\rightarrow$   $I(\text{ADC}\#) \leftarrow I(\text{ADC}\#)+1$   
Accumulated  $I(\text{ADC}\#)$  = Pulse (signal) height spectrum

# Digital Event Data Stream

Example of event stream with signals (observables) measured in 3 inputs of Data Acquisition Module (DDC-8), Sample displays 6 successive events.

Event#	Input 0 Channel #	Input 1 Channel #	Input 2 Channel #	
51	1542	0	0	
52	1530	0	3	Coincident event 0 .AND. 2
53	1486	0	0	
54	1789	256	0	Coincident event 0 .AND. 1
55	1547	0	0	
56	1533	0	0	

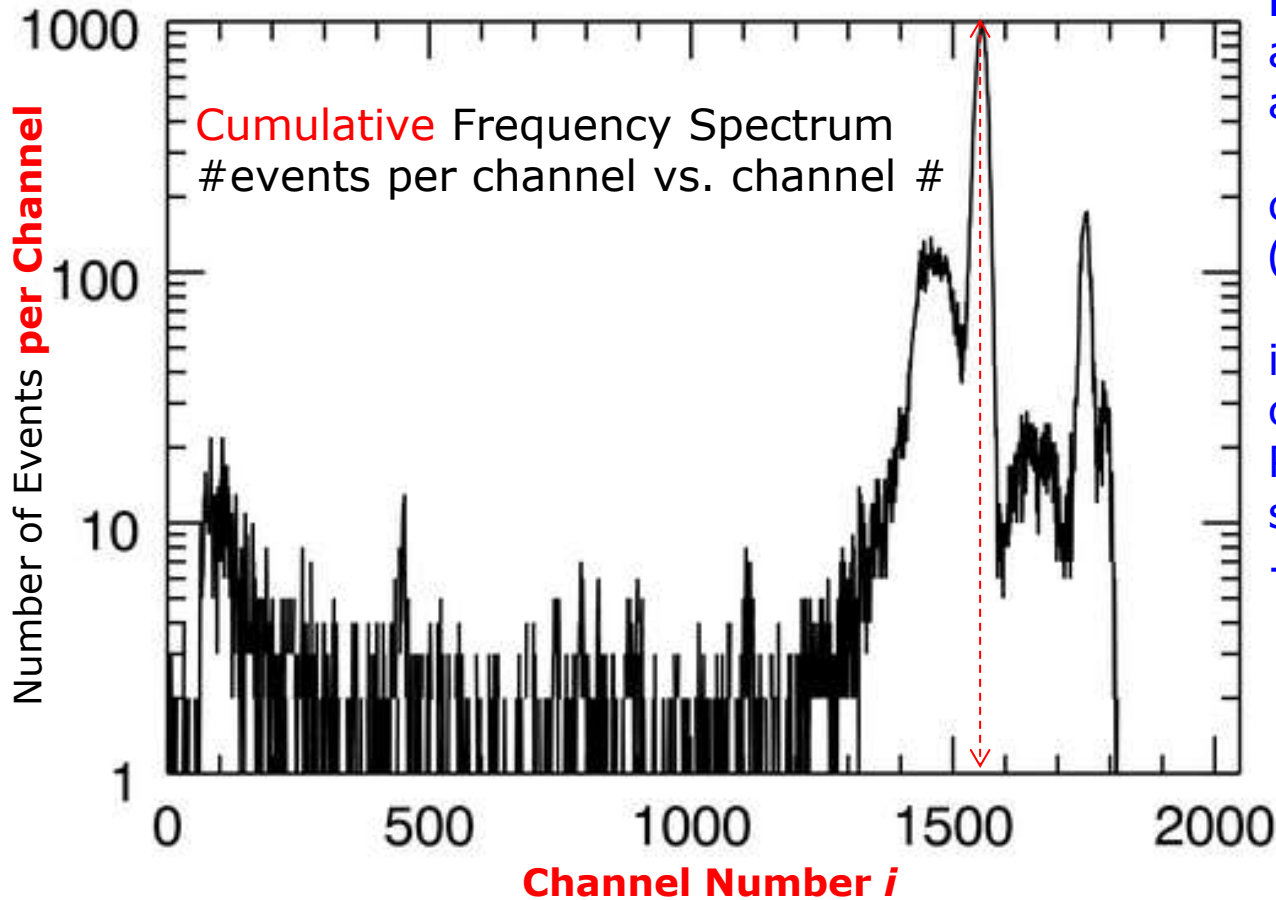
Single event "wave 0" (bracketed above events 51-56)

Single event "wave 1" (bracketed above events 54-55)

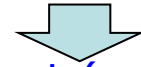
Single event "wave 2" (bracketed above events 51-52)

...and so on

# Histogram of Pulse-Height (Amplitude) Spectrum



Each event provides 1 analog signal amplitude  $V_{in} \rightarrow$   
 $\rightarrow$  digitize  $V_{in}$   
 channel numbers  $i(V_{in})$   
 (segment of PC memory)



increment (add +1)  
 content ( $N_i \rightarrow N_i + 1$ ) of  
 PC cell # = start of  
 spectrum + channel # $i$ .  
 $\rightarrow$  Frequency Histogram

Calibrations :

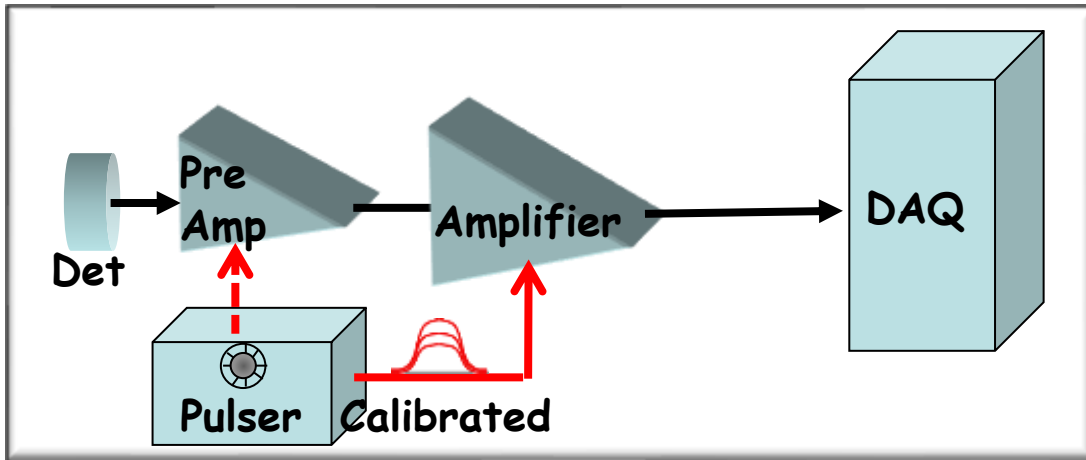
$$i(V) = i_0 + \frac{\Delta i}{\Delta V} \cdot V$$

$$E(i) = E_0 + \frac{\Delta E}{\Delta i} \cdot i$$

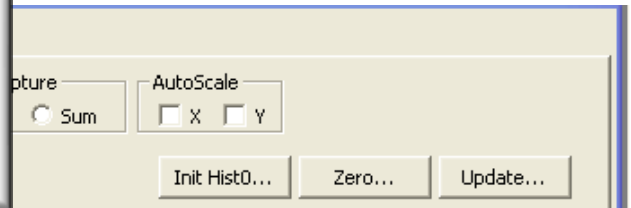
Measured :  $\frac{\text{Number of events } \Delta N}{\text{ADC - channel}} \left( \text{unit} = \frac{\text{counts}}{\text{channel}} \right) \rightarrow \frac{dN}{dE} \left( \text{unit} = \frac{\text{counts}}{\text{keV}} \right)$

Total number of events :  $N = \sum_{i=1}^{2k} \left( \frac{\text{Number of events } \Delta N_i}{\text{ADC - channel}_i} \right) \rightarrow \int_0^{\infty} \left( \frac{dN}{dE} \right) dE$

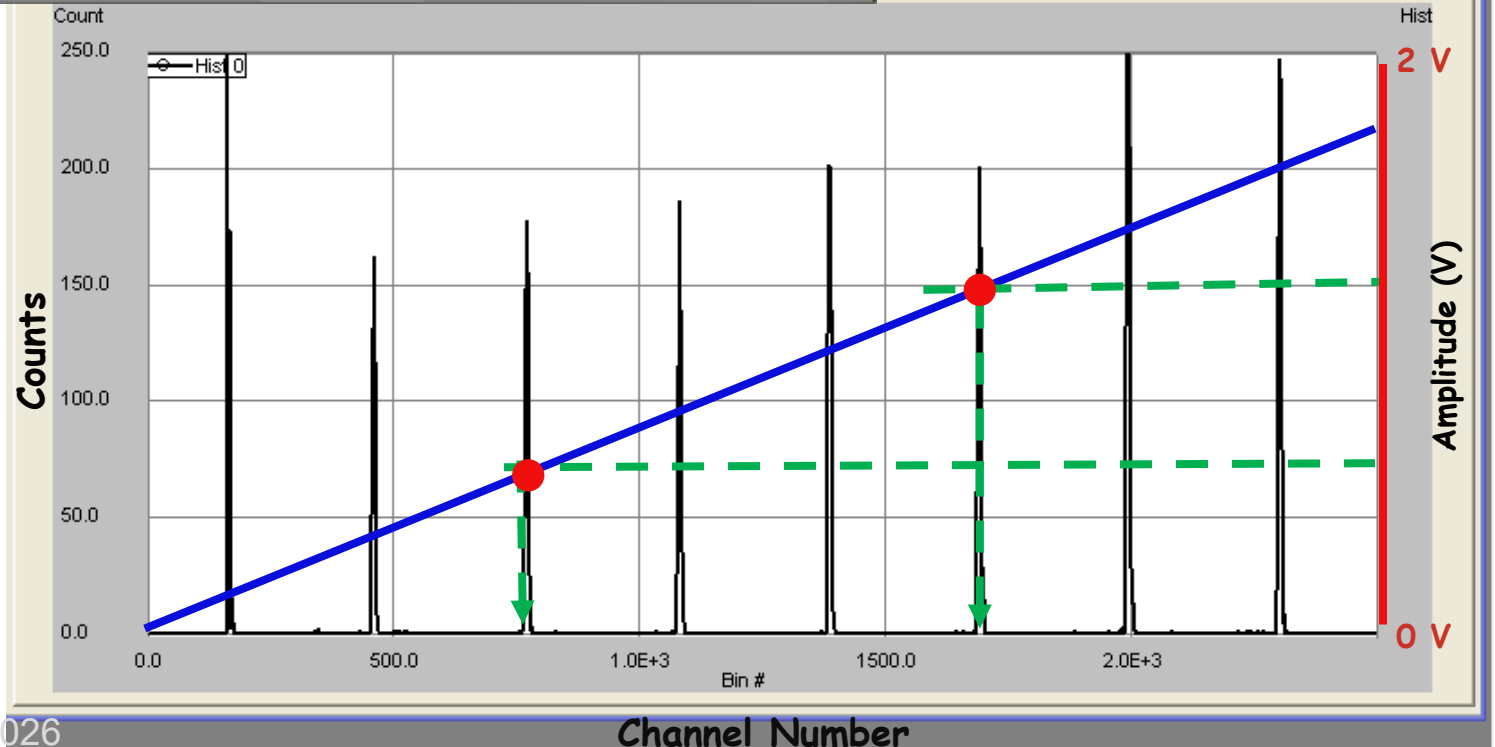
# Amplifier/ADC Linearity Check: "Pulser Calibration"



Series of signals from calibrated **precision pulse generator** fed into slow circuit.



"Pulser Fence" calibrates abscissa of DAQ (Channel, Bin#) in Volts, MeV, etc.



# Precision Pulse Generators



Popular ORTEC spectroscopy-grade precision pulse generators. Other brands: BNC, Tennelec, Canberra,...

Output signal amplitude is highly stable and varies linearly with dial/switch settings.

Output pulse amplitude is calibrated independently in units of Volts, keV, etc.

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# End of Intro Signal Processing